The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
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* DEVICES MAY BE MARKED TMS5502. THE TMS5502 AND TMS9916 ARE COMPLETELY IDENTICAL TO EACH OTHER

* TMS 9916 BUBBLE MEMORY CONTROLLER

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1. INTRODUCTION

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1.1 DESCRIPTION

The TMS 9916 is an MOS/LSI circuit designed to interface between a CPU and a magnetic-bubble memory. It keeps track of the location of data in the bubble memory, under control of the CPU, and stores and retrieves the data. Figure 1 shows a block diagram of the TMS 9916 in a TMS 9900 system.

Bubble memories provide from 20 K bits to over 100 K bits of non-volatible storage. They are organized as up to 1023 parallel circular shift registers, called "minor loops" each of which can be up to 1023 bits long. At one bit location, on each minor loop, bubbles can be transferred to or from another circular register called the "major loop". Data is written into and read from this "major loop" in serial fashion. See Figure 2.

It is the function of the TMS 9916 to keep track of the location of data in the major and minor loops, from an arbitrary "zero" location, and control transfer of data to and from these loops.

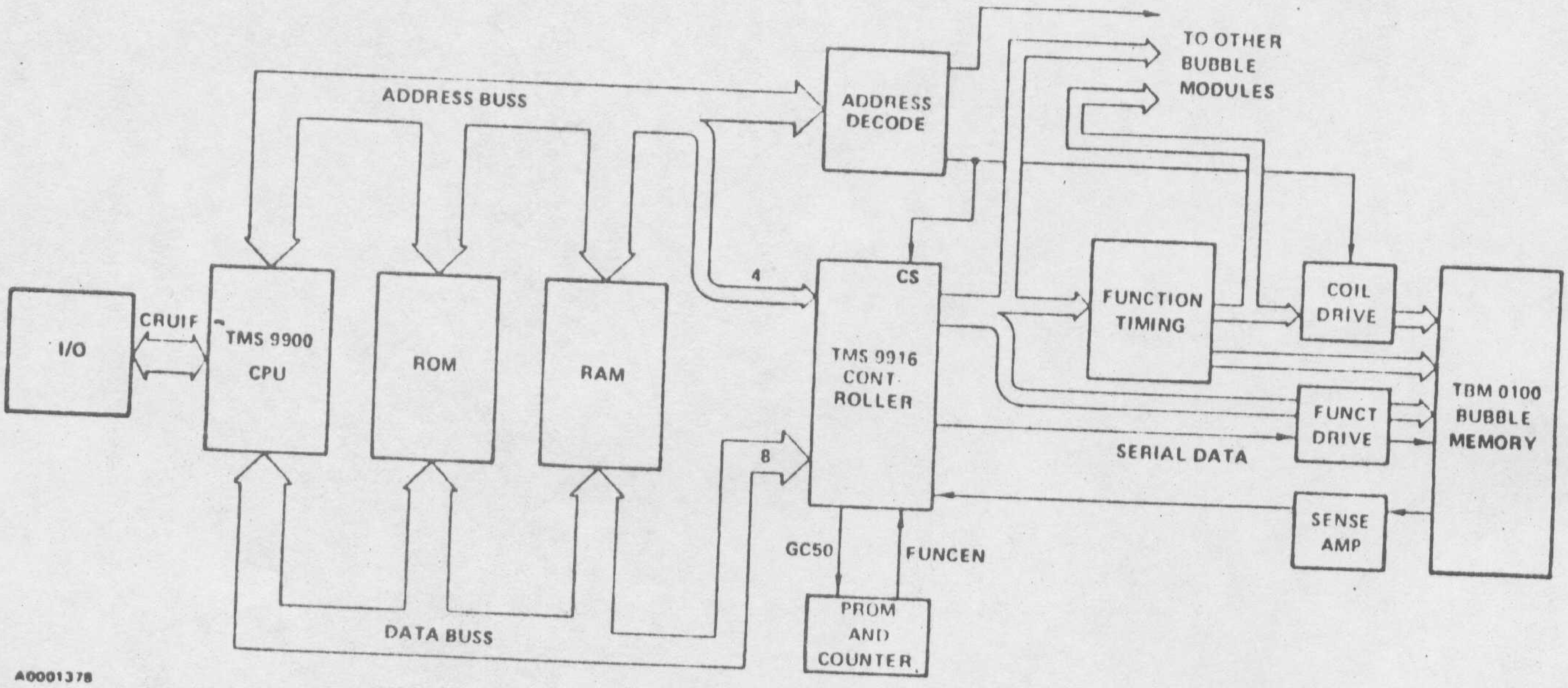

FIGURE 1 – TMS 9916 CONTROLLER IN TMS 9900 SYSTEM

1.2 KEY FEATURES

- Compatible with TMS 9900 Family and TMS 8080 Microprocessors
- Byte oriented transfer of data
- 20 bytes of on-chip buffer storage
- Programmable page size
- Capable of ignoring bad bubble loops
- 50 K bit data transfer rate

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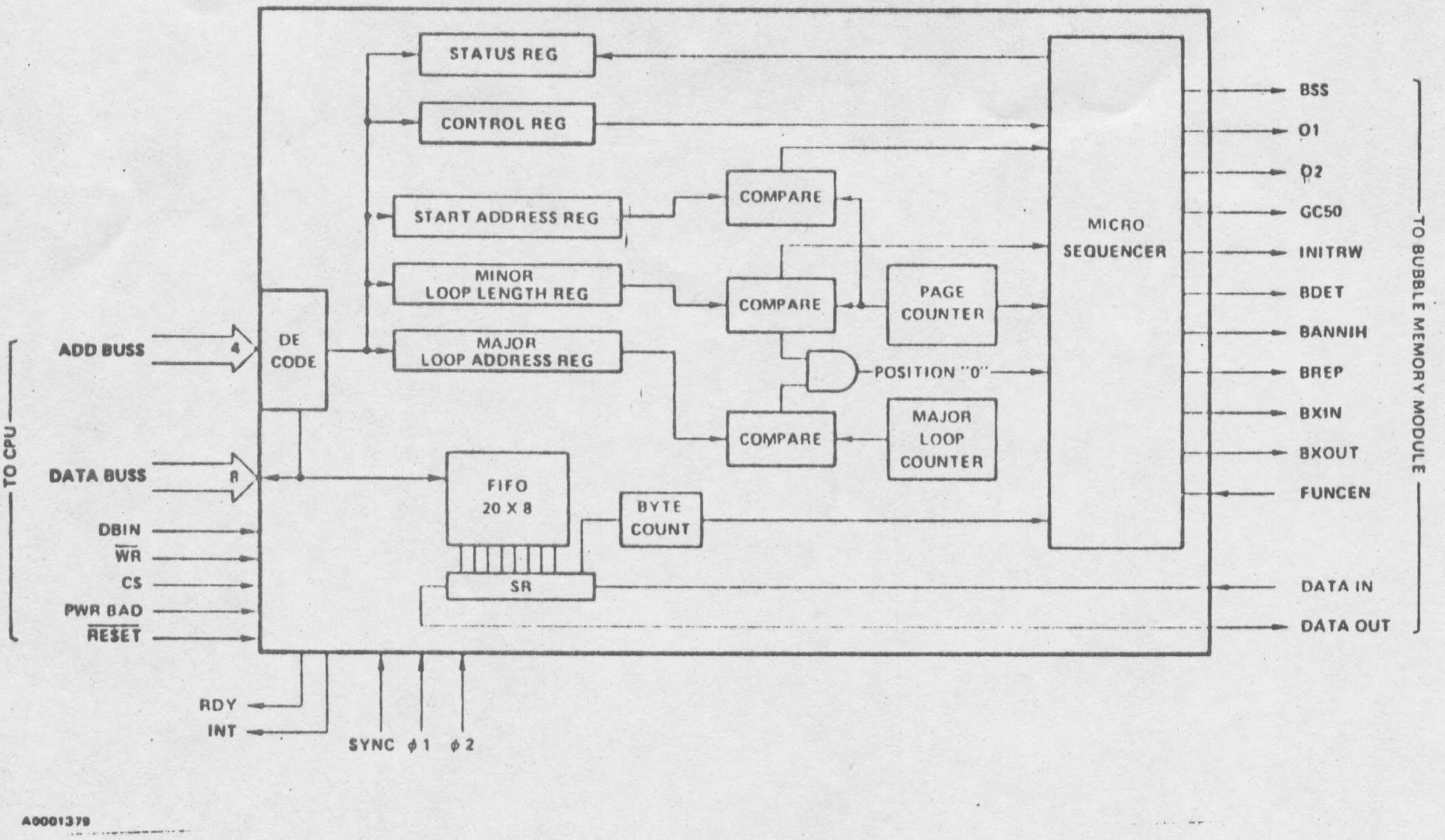

FIGURE 2 – SIMPLIFIED BLOCK DIAGRAM

- 2ϕ clock
- Single- or multi-page mode
- N-channel self-aligned gate MOS technology

2. OPERATION

Operation is controlled by a microprogram contained in an on-board ROM and by the contents of registers set up during initialization by the programmer. A multi-page mode is available which enables loading or unloading the memory in blocks of up to the entire contents of memory.

2.1 ADDRESS AND CONTROL

The TMS 9916 controller is a memory-mapped device and occupies 16 consecutive locations in memory. Each of the first 15 addresses perform a specific function, such as loading a command or loop-size register, reading a status, performing a test, or initiating reading or writing of data. The 16th address (F_{16}) performs no operation. Table 1 lists these addresses and their functions while Table 2 lists the control command bit definitions. Actual location in memory, i.e., the more significant hex addresses, would depend on a decoded address enabling chip select (CS).

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TABLE 1. ADDRESS FUNCTIONS

ADDRESSES (A0–A3)	DATA COMMANDS	OPERATION
0	Load Page Select Reg 1	Write LSB
1	Load Page Select Reg 2	Write MSB
2	Load Control Command Register	Write (see Table 2)
3	Read Byte	Read FIFO
4	Write Byte	Write FIFO
5	Read Status	Read
6	Page Counter 1	Read/Write LSB
7	Page Counter 2	Read/Write MSB
8	Load Minor Loop Size Reg 1	Write LSB
9	Load Minor Loop Size Reg 2	Write MSB
A	Page Position Counter 1	Read/Write LSB
B	Page Position Counter 2	Read/Write MSB
C	Load Page Size Reg	Write
D	Read ROM Byte	Read & Incr. Pointer
E	Read/Write State Address	Read ROM ADDR Reg

NOTE: Address decode F will cause no action by the controller.

TABLE 2. CONTROL COMMAND BIT DEFINITION

BIT NO.	CONTROL COMMAND	RESET FUNCTION	FUNCTION
0	Initialize	System* + CRRST**	"Cold Start" initialization
1	Read Page	System + CRRST	Read page from bubble memory into FIFO page buffer
2	Write Page	System + CRRST	Write page from FIFO page buffer into bubble memory
3	Single Page Mode	Bit 4 = "1"	Sets up controller for single page transfers
4	Multi-Page Mode	System + Bit 3 = "1"	Sets up controller for multi-page transfers
5	Test Mode	System + Bit 5 = "0"	Enables control ROM verification
6	Reset		Software System Reset (Pulse)
7	Interrupt Mask	System + Bit 5 = "0"	Resets Interrupt Level (Pulse)

*System = Software Reset + Hardware Reset

**CRRST is a discrete control bit in the Control ROM.

2.2 STATUS REGISTER

Controller status is maintained in this register and can be read by the microprocessor. Table 3 lists these status conditions.

The following gives a detailed description of each bit:

Controller Busy – A logic "1" indicates that the controller is in the process of reading or writing data to the bubble module. A logic "0" indicates that the controller is in its idle state (State 0).

Load/Incr – A logic "1" indicates that the controller reached its present state by a branch condition. A logic "0" indicates the present state was reached sequentially from the previous state. This bit is updated on each state transition. (Used for testing.)

Inhibit – Indicates that the controller is in a state where transitions out are inhibited until the major loop shift counter goes to zero. (Used for testing).

Byte Read/Written – In the multi-page read mode, this bit indicates the FIFO buffer has been loaded with a byte of data and is ready for reading by the microprocessor. In the multi-page write mode, this bit indicates that the FIFO buffer has been transferred to the bubble data register and is ready to accept new data from the microprocessor. Byte RD/WR will be set every 160 μs (minimum). This status bit is reset when state is ready by the microprocessor.

Page Read/Written – This bit is utilized to indicate that a page of a data has been read into or written out of the FIFO buffer. This status bit is reset when status is read by the microprocessor. This bit is used for testing.

Page Count Zero – Set when the page counter counts to zero. Reset when the Page Count register is re-loaded. This bit indicates that the desired number of pages has been transferred by the controller.

Addressed Page Available – This bit indicates that the page select register is equal to the page position register. Status bit is reset when the status register is read by the microprocessor. This bit is used for testing.

NOTE

Since many of the status bits are reset on reading of the status register, there will be no conflict in setting and resetting the bits (i.e., the bit is set on a different clock phase than it is reset).

TABLE 3. STATUS CONDITIONS

BIT	CONDITION	SET FUNCTION	RESET FUNCTION
0	Page Read/Written	Page Size Counter	Status Read SRST
1	Load/INCR	Updated on State Transition	
2	Inhibit	Updated on State Transition	
3	MLSC Zero	Major Loop Shift Counter = 0	Status Read SRST
4	Addressed Page Available	Comparator	Status Read SRST
5	Controller Busy	Leaving State 0	"1" to "0" transition of BSS
6	Page Count Zero	Page Count Register	Page Count Register Loaded
7	Byte Read/Written	Byte Counter	Status Read SRST

2.3 TMS 9916 PIN DESCRIPTION

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Table 4 defines the TMS 9916 pin assignments and describes the function of each pin.

TABLE 4. TMS 9916 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
V_{BB}	1	I	−5 volt supply
B_{SS}	2	O	Bubble start shift, used to start and stop bubble field drive clocks
GC50	3	O	Gated 50 kHz clock synchronous with the data transfer rate out of the bubble module
O1	4	I	Timing signals to the function timer
O2	5	I	
RSET	6	I	Initialization signal which resets the following functions: 1) Status register (except page count zero, which is set) 2) ROM function latch 3) Byte counter 4) Interrupt 5) Output Buffer 6) Control signals 7) ROM address register 8) Flags – multipage, initialize, read page, write page 9) Page count register 10) Page-select register 11) Byte select 12) Clock distribution
V_{DD}	7	I	+12 volt supply voltage
$\overline{WR}$	8	I	Write signal to the controller indicating that the processor is executing a write instruction
RDY	9	O	Signal generated by the controller to allow commands from the processor
SYNC	10	I	Synchronization signal to the controller indicating that a command sequence is starting (see Note 2).
CS	11	I	Chip select to the controller which enables the command decode logic
A3	12	I	Four address lines used for encoding commands to the controller.
A2	13	I	
A1	14	I	
A0	16	I	
V_{CC}	15	I	+5 volt supply
DBIN	17	I	Data bus in signal to the controller, indicating the processor is executing a read instruction

TMS 9916 PIN ASSIGNMENTS

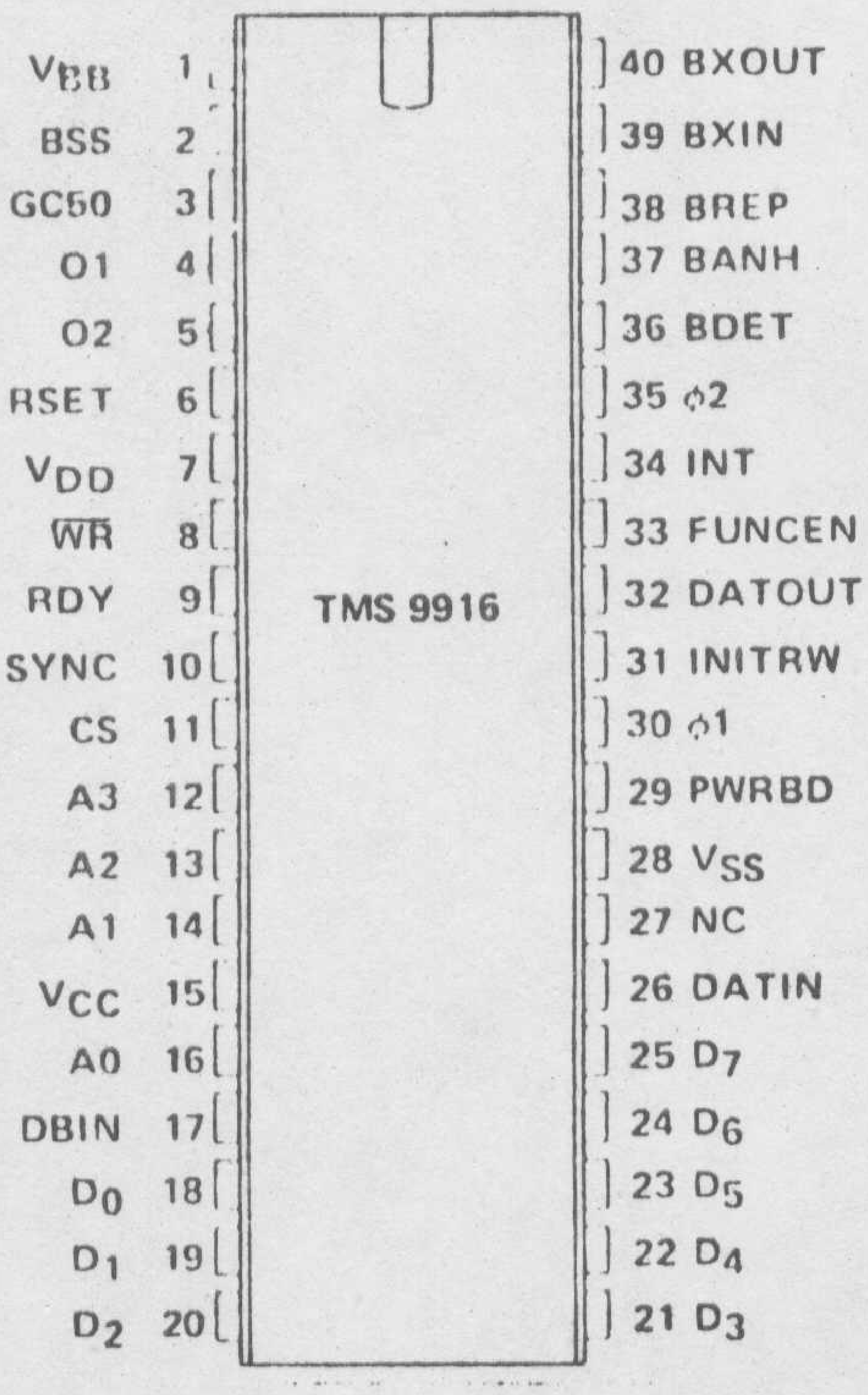

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TABLE 4. TMS 9916 PIN ASSIGNMENTS AND FUNCTIONS (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
D0	18	I/O	Data is transferred to and from the processor over this bidirectional data bus
D1	19		
D2	20		
D3	21		
D4	22		
D5	23		
D6	24		
D7	25		
DATIN	26	I	Serial data from the bubble module to the controller
	27		No connection
V_{SS}	28	I	Ground
PWRBAD	29	I	Power bad signal to the controller indicating that the power source has been interrupted and an orderly shutdown should be initiated. This permits the controller to circulate the memory to its zero address, for a known starting point on power up.
$\phi1$	30	I	Two phase 2 MHz clock which governs all of the controller timing sequences
$\phi2$	35	I	
INITRW	31	O	Initiate read-write signal from the controller indicating that it is about to read from or write to the bubble module
DATOUT	32	O	Serial data from the controller to the bubble module
FUNCEN	33	I	Function enable to the controller, generated by the PROM, used to inhibit data shifting when there is a bad minor loop in the bubble memory
INT	34	O	Signal generated by the controller to the processor indicating data is ready to be read or written.
BDET	36	O	Bubble detect enable to the bubble module, indicating that a bubble passing the detector and should be read
BANH	37	O	Bubble annihilate signal from the controller, indicating that bubbles in the annihilate position in the major loop should be collapsed (see Note 1)
BREP	38	O	Bubble replicate signal from the controller indicating that the bubble located at the replicate position in the major loop should be split into two bubbles. One continues along the major loop, the other travels towards the detector (see Note 1)
BXIN	39	O	Transfer in enable, indicating that bubbles in the major loop are to be transferred to the minor loops (see Note 1)
BXOUT	40	O	Transfer out enable indicating that bubbles in the minor loops are to be transferred to the major loops (see Note 1)

NOTES: 1. Transfer of a bubble between major and minor loops, and from major loop to read area is a destructive process; that is the bubble transferred is "annihilated". The replicate signal enables the bubble to be split as it heads for the read area, so that it can continue around the major loop, eventually to be restored to its proper position in a minor loop.

2. In applications where a seperate SYNC signal is not available, SYNC and CS may be tied together.

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3. TMS 9916 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage, V_{CC} (with respect to V_{BB})	−0.3 to 20 V
Supply voltage, V_{DD} (with respect to V_{BB})	−0.3 to 20 V
Supply voltage, V_{SS} (with respect to V_{BB})	−0.3 to 20 V
Input voltages (with respect to V_{BB})†	−0.3 to 20 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

†For all combinations of inputs, the I/O lines may be shorted to V_{SS} or V_{CC} for a period not to exceed five (5) milliseconds without any damage to the device.

3.2 RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to 70°C

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage, V_{BB}	−5.25	−5	−4.75	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High level input voltage, V_{IH} (all inputs except clocks)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{\phi H}$	9		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks)	−1		0.8	V
Low-level clock input voltage, $V_{\phi L}$	−1		0.6	V

3.3 STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current (all inputs except clock and data I/O)	V_I = 5 V			100	μA
I_{IH}	High level data I/O input current	V_I = 5.25 V, CS = 0			100	μA
I_{IL}	Low-level data I/O input current	V_I = 0, CS = 0			−100	μA
I_{BB}	Supply current from V_{BB}				−1	mA
I_{CC}	Supply current from V_{CC}				75	mA
I_{DD}	Supply current from V_{DD}				35	mA
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = 400 μA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 5.25 V, I_{OL} = 1.9 mA			0.4	V
C_i	Capacitance, all input except clock				10	pF
$C_{i(\phi)}$	Capacitance, clock input				50	pF
C_o	Capacitance, output buffers				25	pF

3.4 OUTPUT LOAD CAPACITANCE

PARAMETERS	CAPACITIVE LOAD
Data Output Buffer (D0 - D7)	100 pF plus 1 TTL load
Function Enable Buffers (BSS, BDET, BAN, BREP, BXIN, BXOUT, DATA OUT)	25 pF plus 1 TTL load
Output Buffers (ϕ1 CLK, ϕ2 CLK, GC50, INTERRUPT, READY, INITRW)	25 pF plus 1 TTL load

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3.5 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	0.48		2	μs
$t_{r(\phi)}$	Clock rise time (10% to 90%)	0		50	ns
$t_{f(\phi)}$	Clock fall time (90% to 10%)	0		50	ns
$t_{w(\phi 1)}$	Pulse width, clock 1	60			ns
$t_{w(\phi 2)}$	Pulse width, clock 2	220			ns
$t_{d(\phi 1-\phi 2)}$	Delay time, clock 1 to clock 2	0			ns
$t_{d(\phi 2-\phi 1)}$	Delay time, clock 2 to clock 1	55			ns
$t_{d(\phi 1-\phi 2)}$	Delay time, leading edges of clock 1 to clock 2	80			ns

NOTE: RESET can occur anywhere but must be held at least two clock cycles.

$T_A = 0^oC$ to $+ 70^oC$

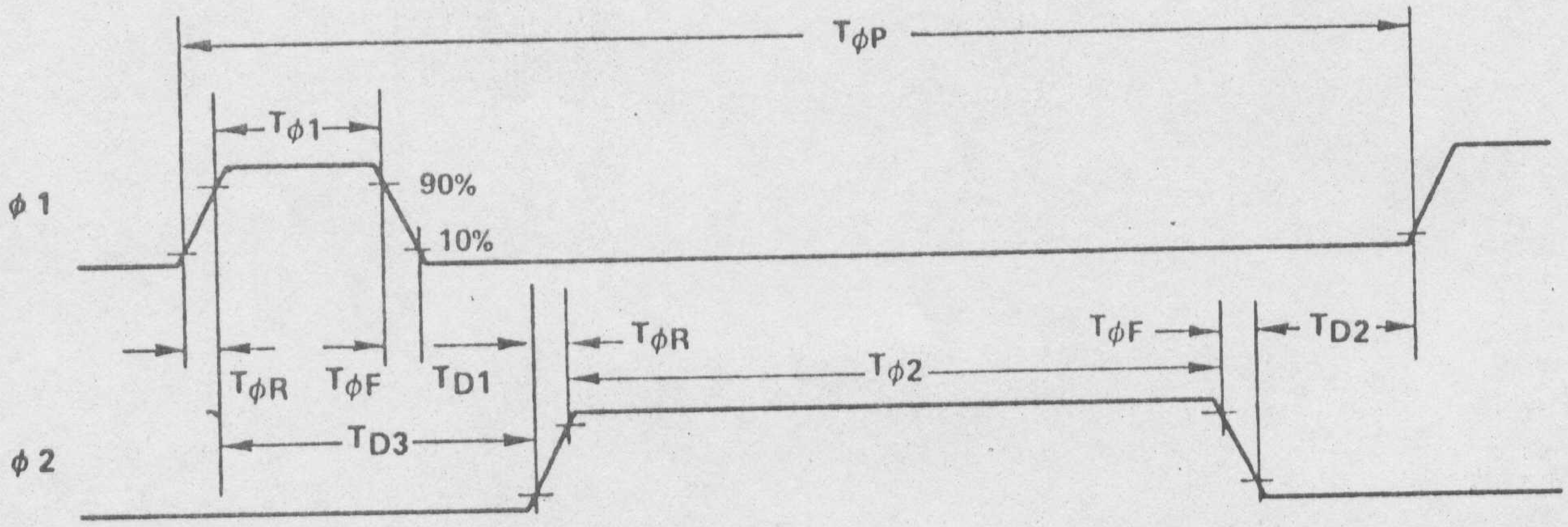

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FIGURE 3 – CLOCK TIMING REQUIREMENTS

3.6 INTERFACE TIMING, $T_A = 0^\circ C$ to $70^\circ C$

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(WR)}$	Pulse width, WR	50			ns
$t_{su(ad)}$	Setup time for address in clock 1	125			ns
$t_{su(CS,S)}$	Setup time for chip select and SYNC in clock 1	105			ns
$t_{su(WR)}$	Setup time for WR input in clock 2	160			ns
$t_{su(da)}$	Data setup time in clock 1	105			ns
t_h	Hold time from clock 1	0			ns
$t_{d(da)}$	Data output delay time from clock 2 to valid			290	ns
$t_{d(da)}$	Data output delay time from DBIN to FLOAT			110	ns
t_d	DBIN input delay time into clock 2			160	ns
$t_{d(R)}$	READY output delay time in clock 2			80	ns
$t_{d(S)}$	SYNC input delay time from clock 1	0			ns
$t_{d(D)}$	Delay time between SYNC "0" to "1" transitions	1.5			μs

NOTE: All timing specifications are in accordance with capacitive loading.

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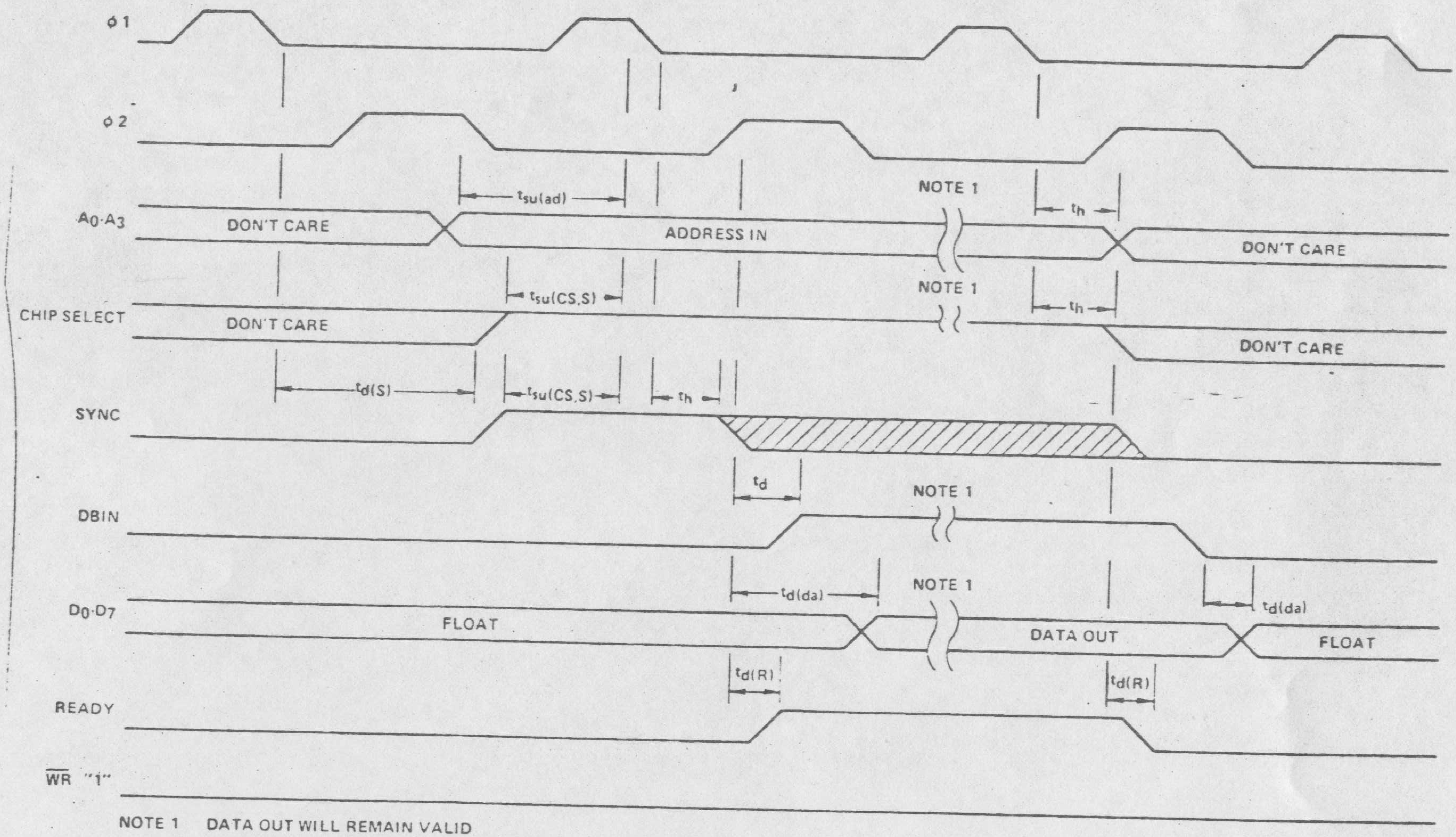

NOTE 1 DATA OUT WILL REMAIN VALID
AS LONG AS ADDRESS AND CS REMAIN VALID.

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FIGURE 4 – READ CYCLE TIMING

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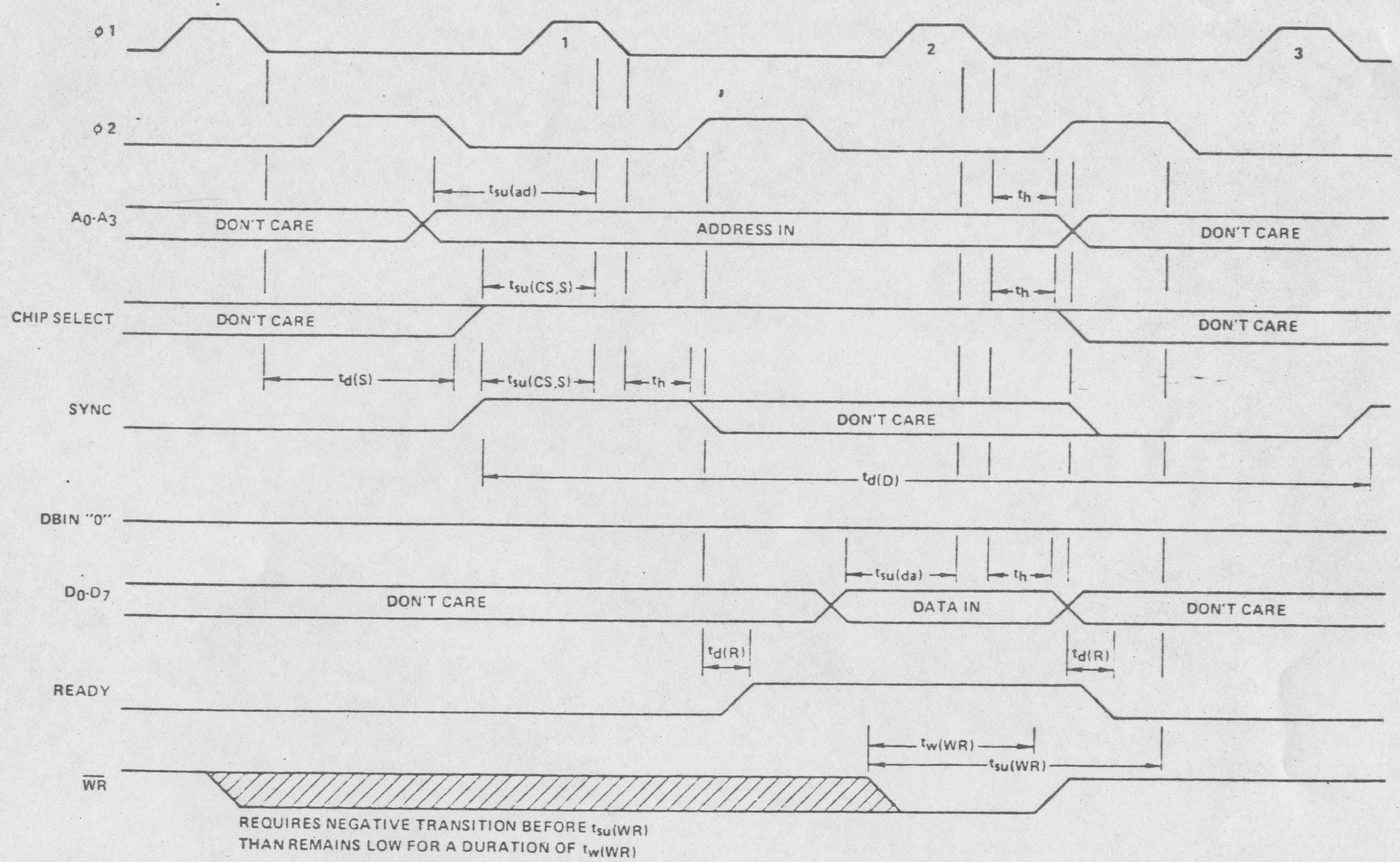

REQUIRES NEGATIVE TRANSITION BEFORE $t_{su(WR)}$
THAN REMAINS LOW FOR A DURATION OF $t_{w(WR)}$

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FIGURE 5 – WRITE CYCLE TIMING

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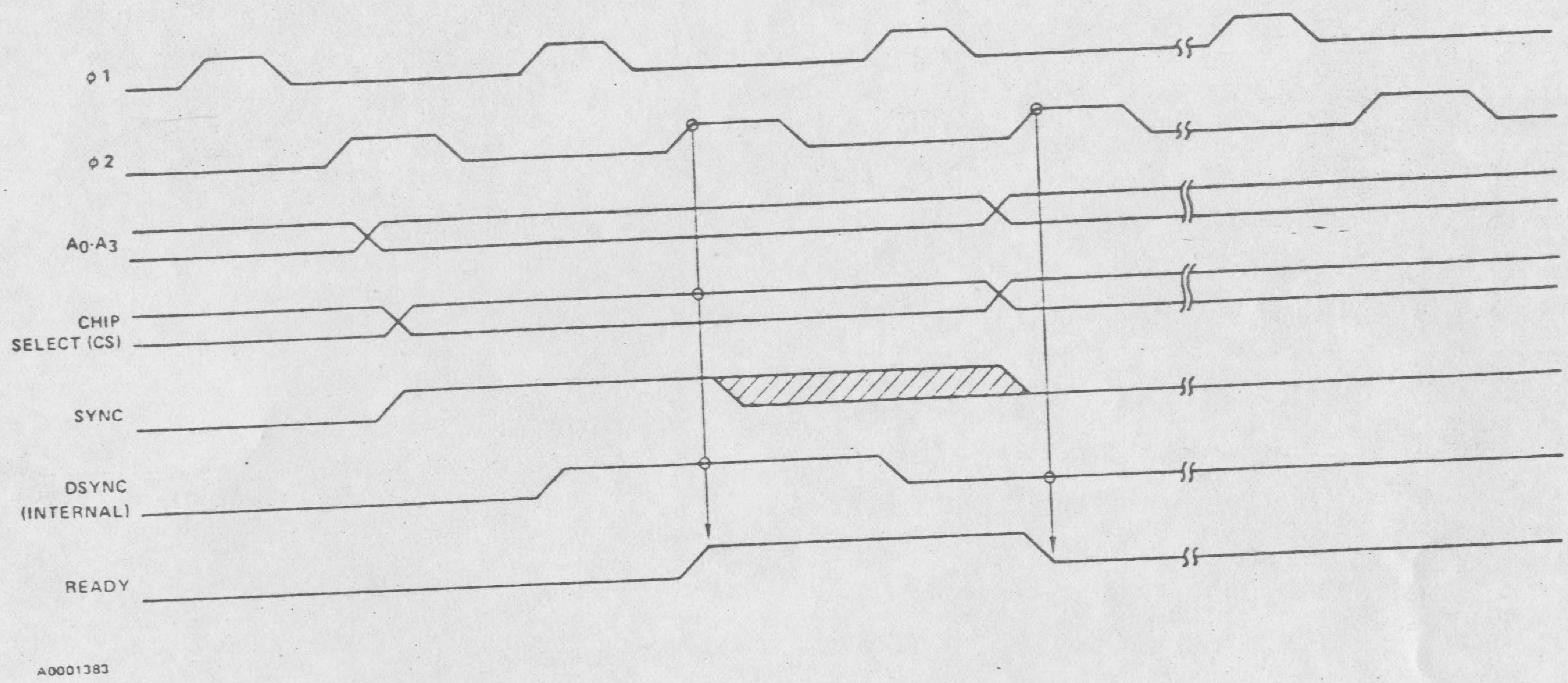

FIGURE 6 – RELATION BETWEEN READY, SYNC, AND CHIP SELECT

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PARAMETER		MIN	TYP	MAX	UNIT
t_w	INITRW pulse width	500		1000	ns
$t_{su(da)}$	Setup time, data input from clock 1			2500	ns
$t_{h(da)}$	Hold time, data input from clock 2	1000			ns
t_d	GC50 delay time from clock 1	0		200	ns
t_d	INITRW delay time from clock 1			200	ns
$t_{d(da)}$	Data output delay time from GC50		350		ns

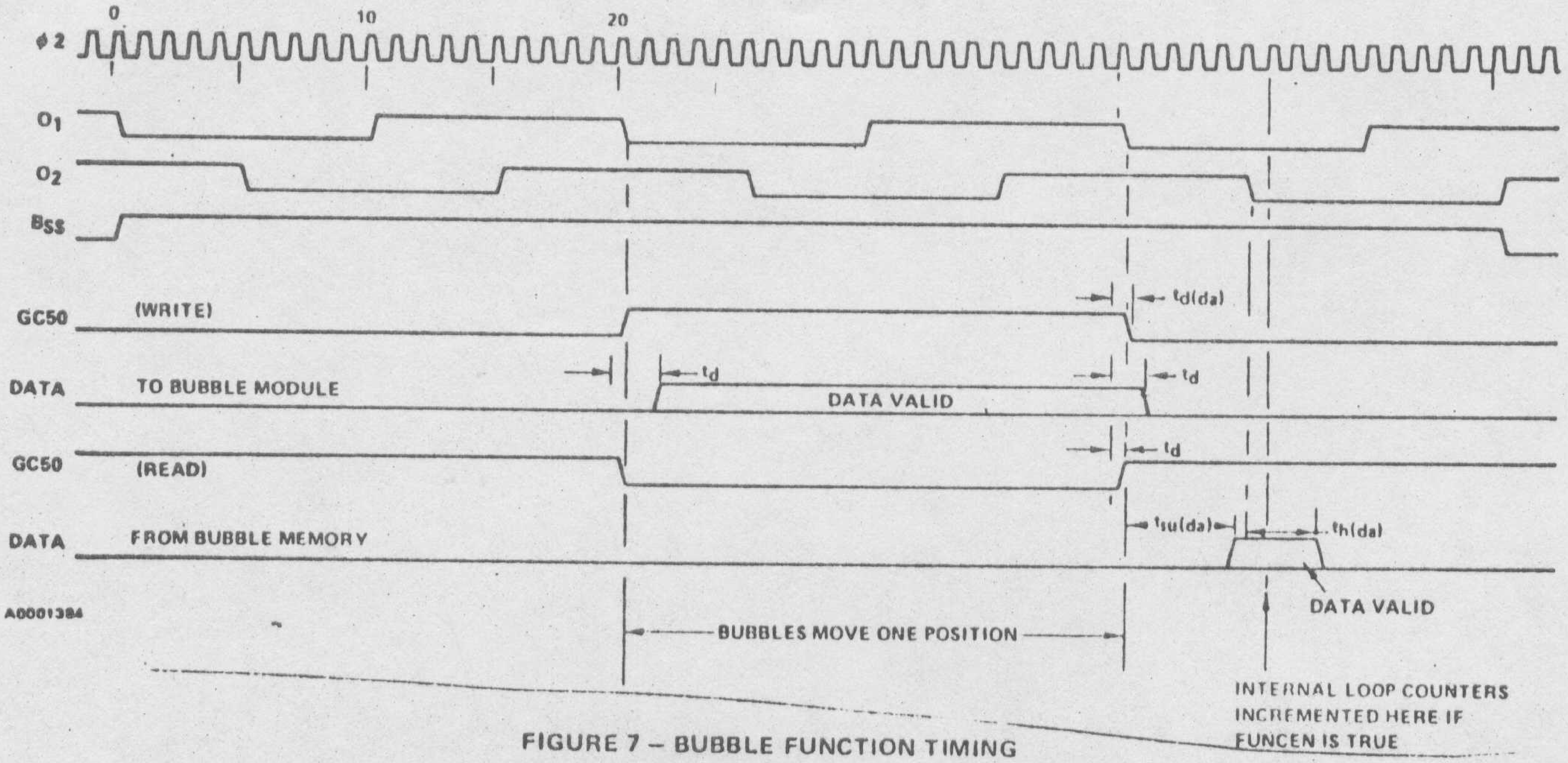

FIGURE 7 – BUBBLE FUNCTION TIMING

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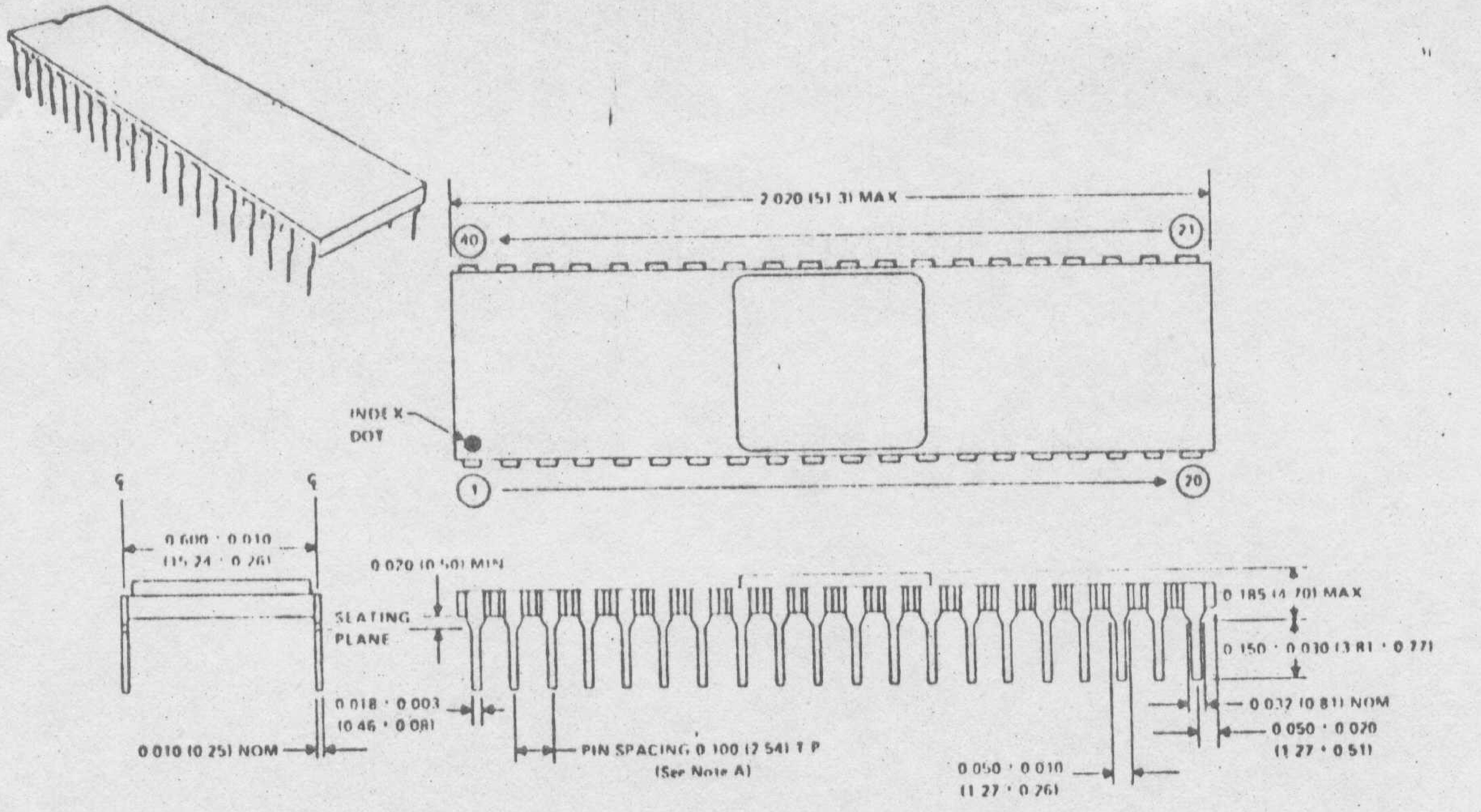
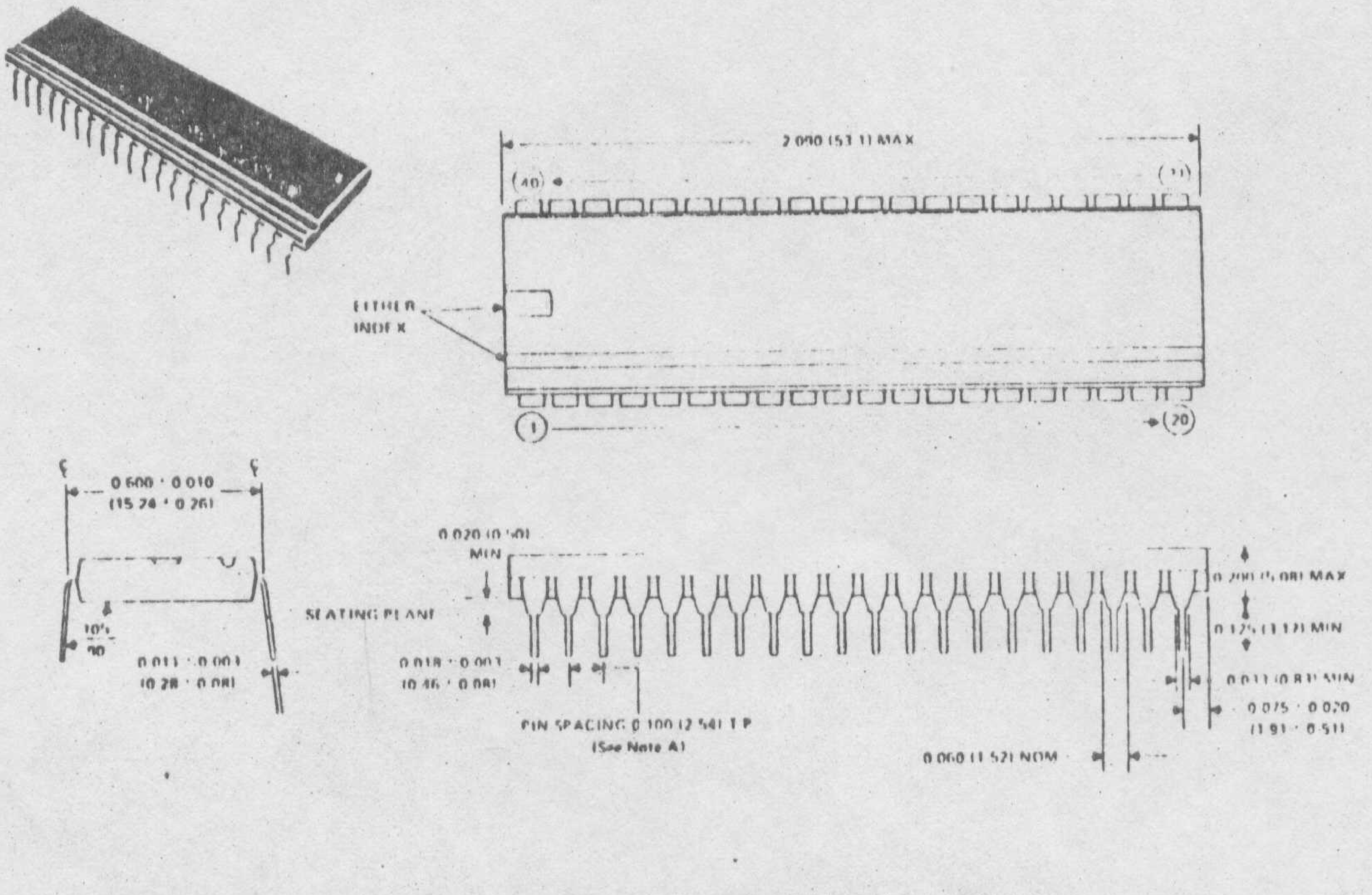
4. MECHANICAL DATA

4.1 TMS 9916 – 40 PIN CERAMIC PACKAGE



NOTES a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

4.2 TMS 9916 – 40-PIN PLASTIC PACKAGE



NOTES a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.